X-721-67-469
PREPRINT

AN AIRBORNE PULSE COUNTER AND SERIAL ENCODER

SEPTEMBER 1967

GSFC

GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

X-721-67-469

AN AIRBORNE PULSE COUNTER

AND SERIAL ENCODER

John W. Fennel
Raymond J. Stattel
John F. Fitz
Marcus L. Moore

Sounding Rocket Instrumentation Section

September 1967

GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland

AN AIRBORNE PULSE COUNTER

AND SERIAL ENCODER

John W. Fennel
Raymond J. Stattel
John F. Fitz
Marcus L. Moore

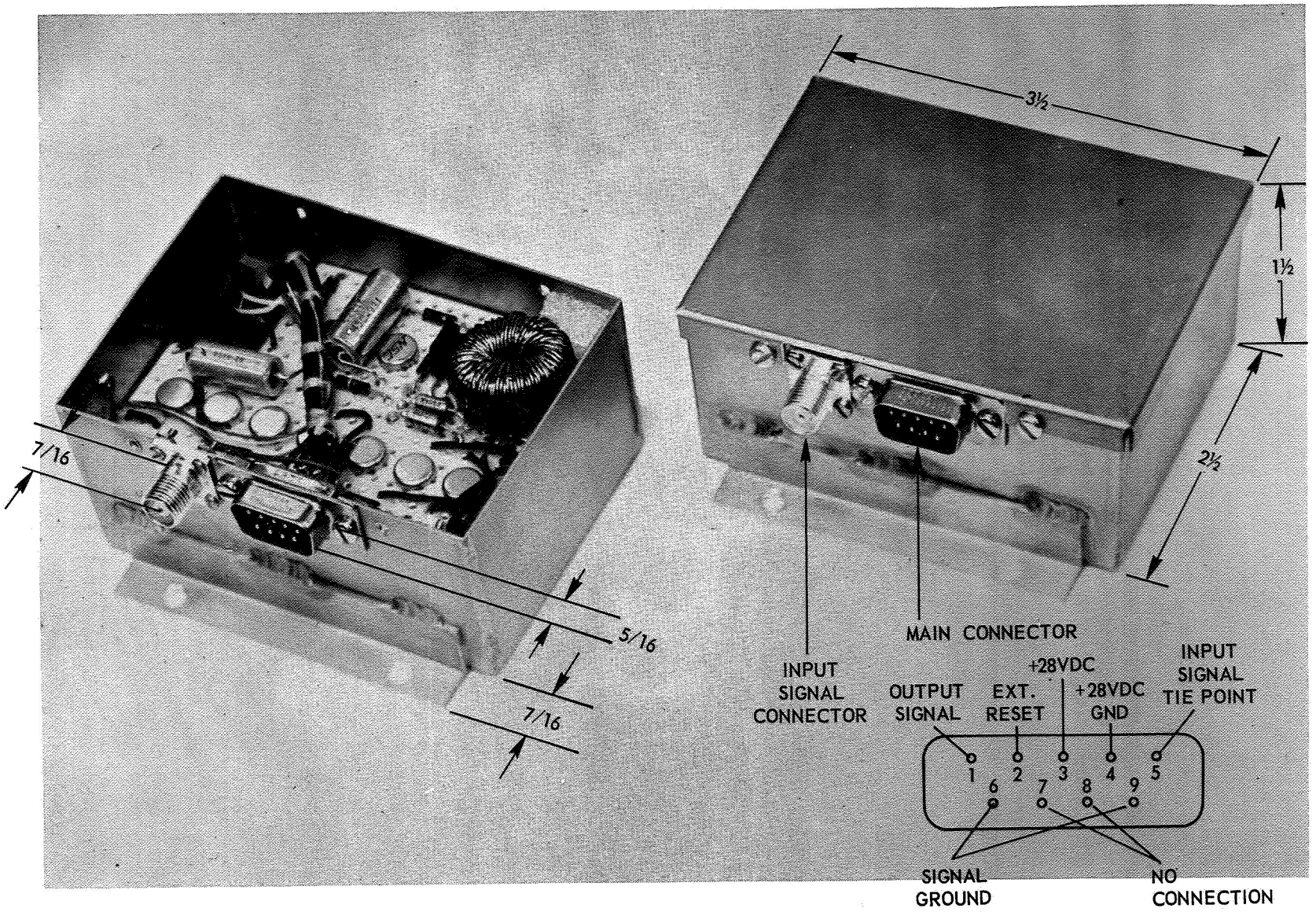
Sounding Rocket Instrumentation Section

ABSTRACT

A compact, self-contained pulse counter and serial encoder capable of counting up to 99,999 and producing a serial binary-coded decimal output is described. The unit was designed to count pulses from a digital accelerometer and produce an output, consisting of the accumulated count, every second. The output may be transmitted over a single low-frequency channel of a standard FM/FM telemeter. The accumulated count is easily read from a real-time analog record and is suitable for digital processing. The device lends itself to applications where the total number of pulses from a sensor is required.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS



Frontispiece. Pulse Counter and Serial Encoder

AN AIRBORNE PULSE COUNTER AND SERIAL ENCODER

INTRODUCTION

The counter-encoder here described was designed and built by the Sounding Rocket Instrumentation Section in response to a request by the Delta Project office. The request was to provide a pulse-counting device to be used, in flight, with a new digital accelerometer, as a part of the third-stage instrumentation system of the Delta launch vehicle, in the forthcoming Anchored IMP E satellite* launching. The third-stage instrumentation system was also provided by the Sounding Rocket Instrumentation Section.

The unit counts pulses from the accelerometer and provides, once per second, a serial binary-coded decimal (BCD) output giving the accumulated count. The output format, indicating a count of 41,062, and a functional block diagram of the counter-encoder are shown in Figure 1. The maximum count accumulation is 99,999. Input pulses must be positive, of 10 to 30 volts in amplitude, and have a rise time of 10 microseconds or less. The unit operates from a 10 to 30 volt d-c battery source.

Since Fairchild RTL micrologic elements were immediately available, they were used throughout. In designing for future fabrication, consideration should be given to the use of dual RTL micrologic elements, which could reduce the size of the unit by as much as a half. The use of low power logic for reduced power consumption should also be considered.

All components of the counter-encoder and its regulator are housed in a metal case, 13.1 cubic inches in volume. The total weight of the unit is about 13 ounces. Power consumption is approximately 9 watts. All circuit components, including those of the regulator, are mounted on three boards of equal size (Figure 2). Non-rigid interconnections between boards permit manipulation of the boards in accordian fashion. This mode of construction provides ease of access to all components and allows insertion of the board assembly into a compact container (Figure 3).

The case (Frontispiece and Figure 3) has external mounting brackets. It is suggested that any future packages use mounting screws inside the case to

---

*This IMP (Interplanetary Monitoring Probe) was successfully launched from Cape Kennedy on July 19, 1967 and successfully injected into lunar orbit on July 22, 1967.

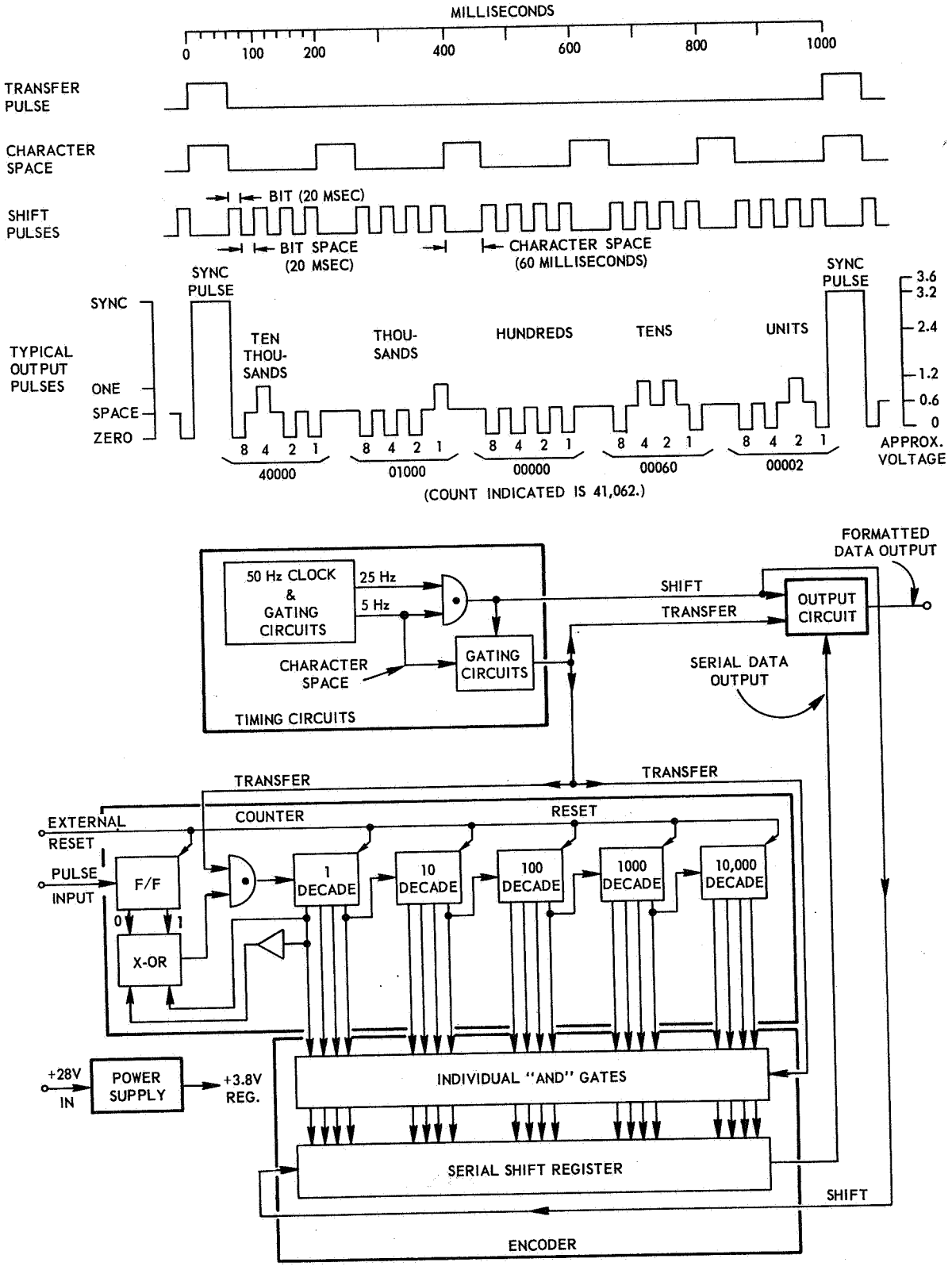
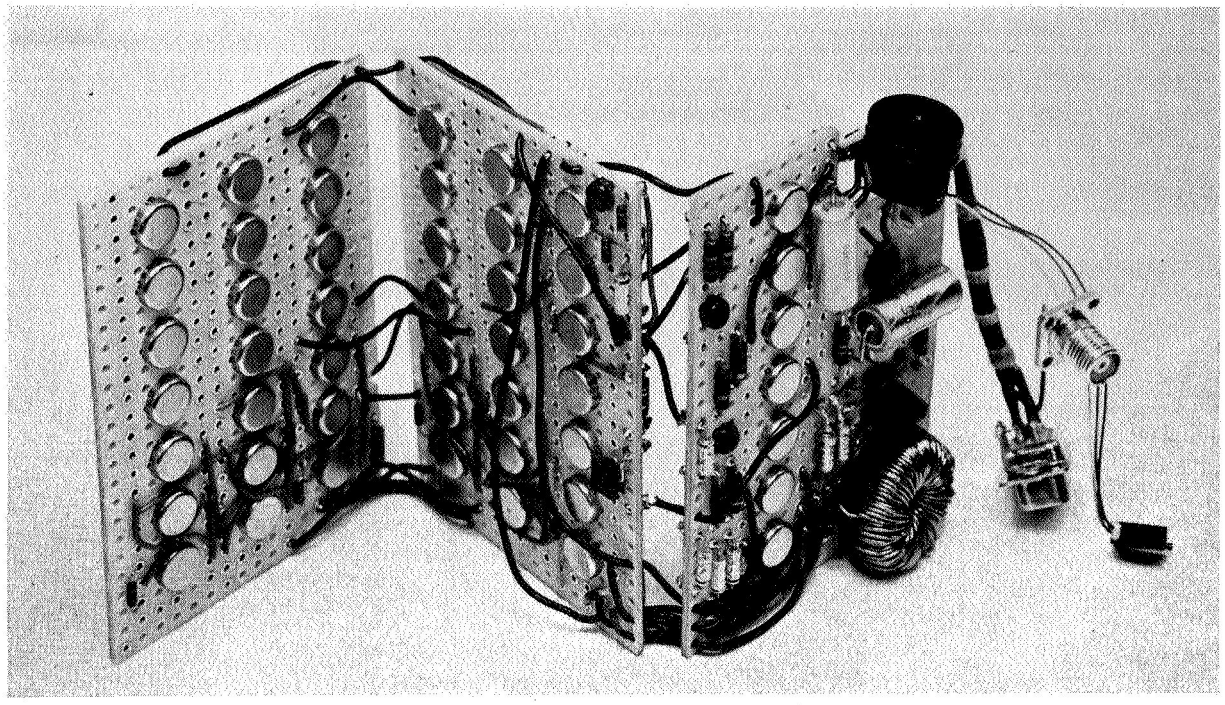
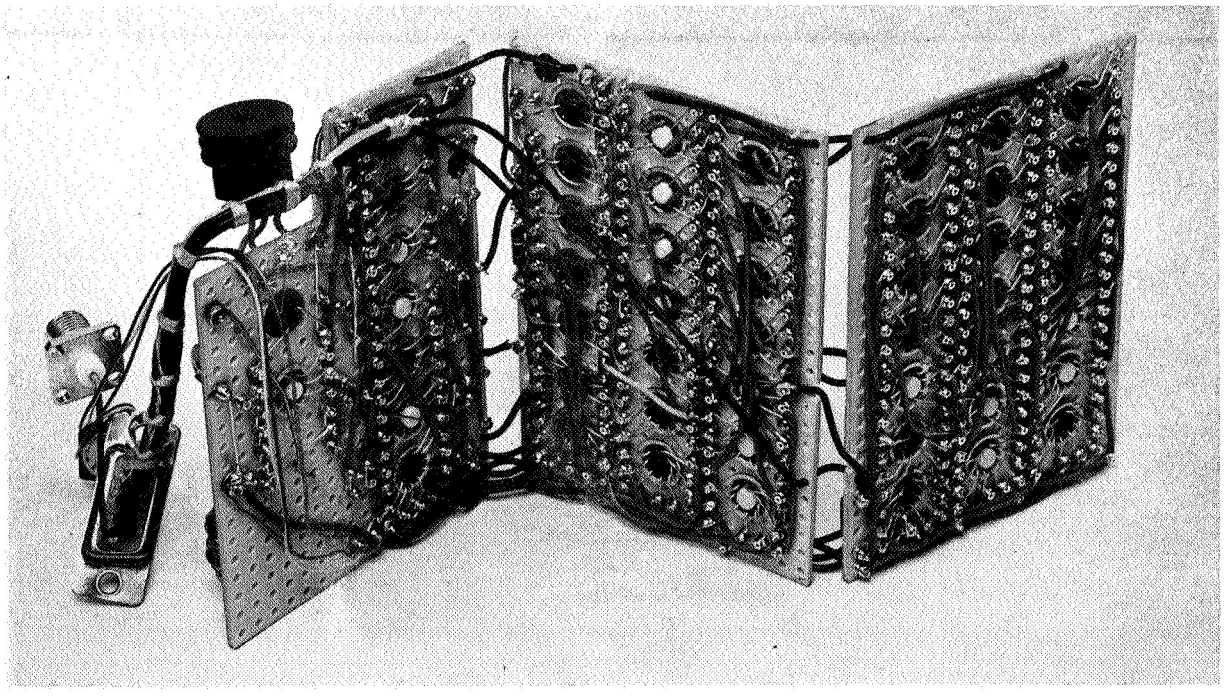


Figure 1. Counter-Encoder Data Format and Block Diagram

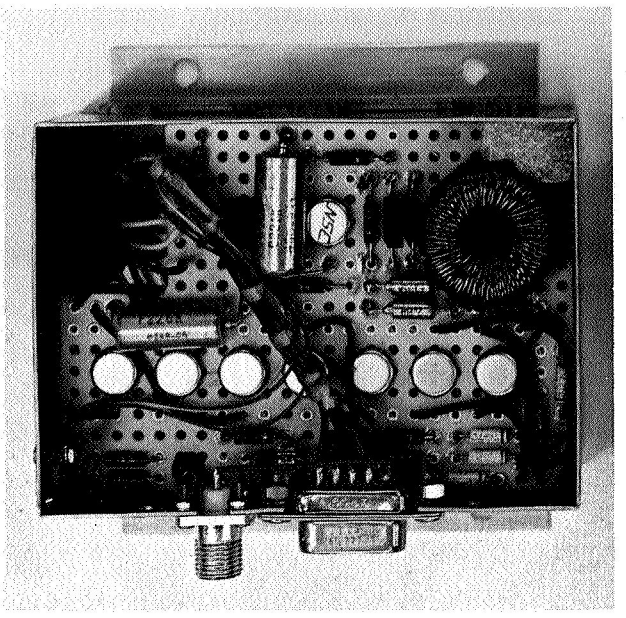


A. Component Side

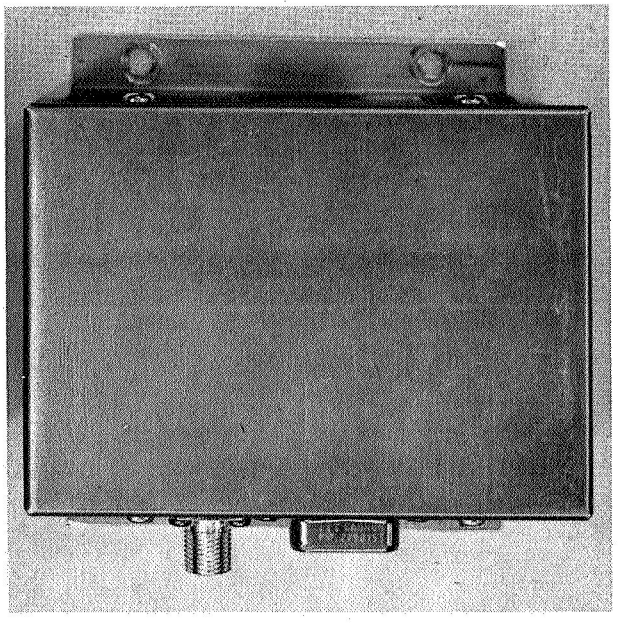


B. Wiring Side

Figure 2. Views of the Board Assembly



A. Board Assembly Installed in Case



B. Counter-Encoder With Cover Installed

Figure 3. Installation of the Board Assembly and Cover

further reduce the overall dimensions. Electrical connections are made through two connectors.

FUNCTIONAL DESCRIPTION

GENERAL OPERATION

Input pulses are applied to a five decade counter which maintains the accumulated count. (See Figure 1.) Once per second, the contents of the counters are transferred in a parallel manner to the shift register, and shifted out in a serial manner, to the output circuit. When the shifting out is finished, new data is instantly (in about 1 microsecond) transferred in.

The timing-pulse generating circuits (timing circuits), the five-decade counter (which holds the accumulating count), the encoder (which contains the shift register), the output circuit, and the regulated power supply constitute the five functional elements of the counter-encoder. Descriptions of the operation of each of these elements follow. In this discussion, reference should be made to the logic diagram of Figure 4. Numbers and reference symbols of the logic diagram are also given in Figures 5 and 6, which show physical locations on the mounting boards.

TIMING CIRCUITS

Timing in the counter-encoder is provided by a clock-pulse generator, an astable multivibrator operating at a normal frequency of 50 hertz. The clock pulses are the source from which the symmetrical BIT, and the nonsymmetrical CHARACTER SPACE, SHIFT, TRANSFER, and SYNC waveforms are derived.

The clock pulses are applied to decade module 5 which divides by 2 and 10 to produce the BIT waveform at 25 hertz, and the CHARACTER SPACE waveform at 5 hertz. The 25-hertz BIT waveform is a square wave establishing a 40-millisecond interval to contain one bit and one bit space. The 5-hertz nonsymmetrical CHARACTER SPACE waveform establishes the basic element of the output format. It consists of 60-millisecond pulses occurring every 200 milliseconds. It serves to establish (1) a 60-millisecond space between each character (decimal digit) of the decimal number, and (2) a 140-millisecond interval to contain the combination of four bits necessary to represent the decimal digits 0 through 9.

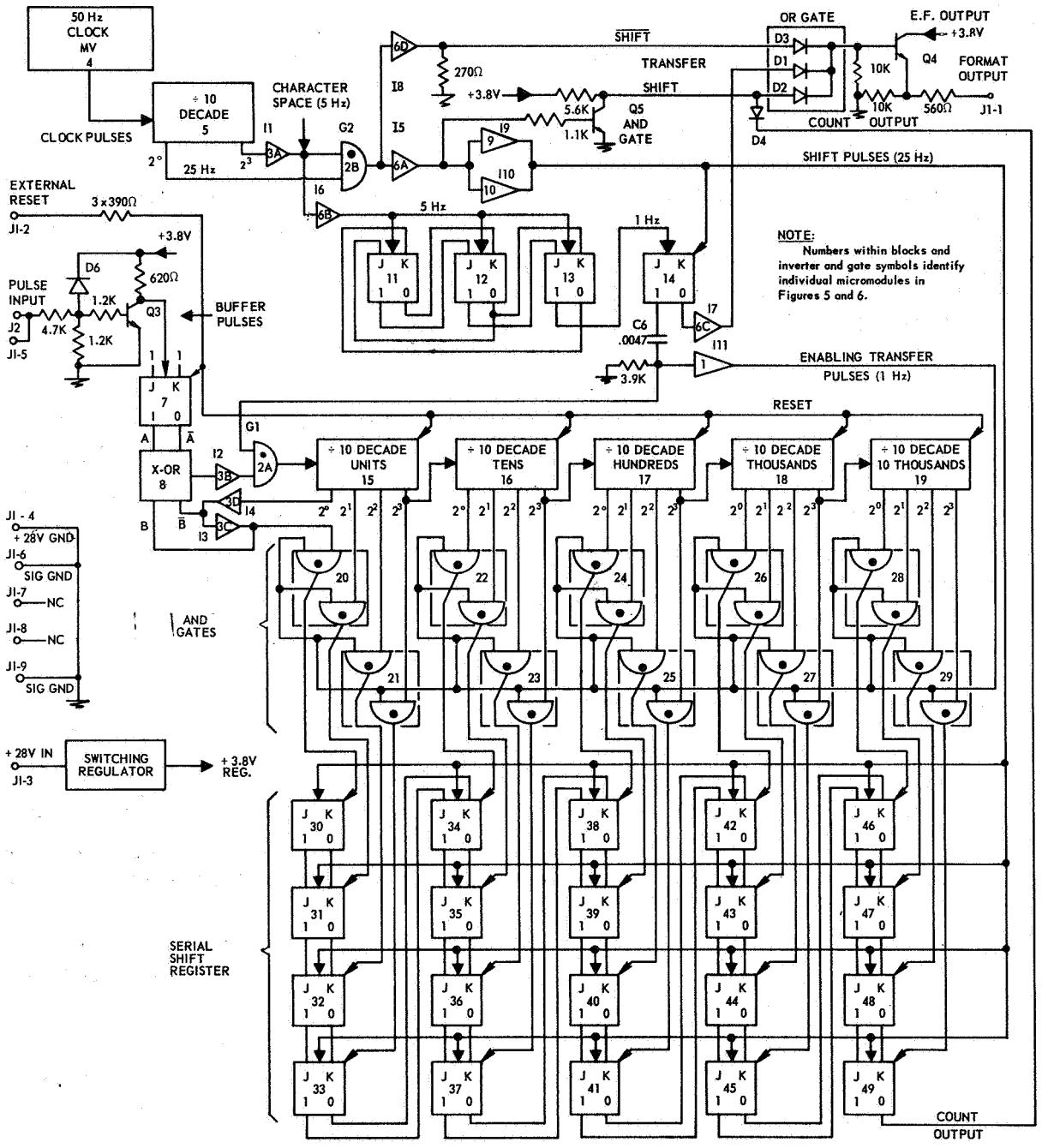


Figure 4. Counter-Encoder Logic Diagram

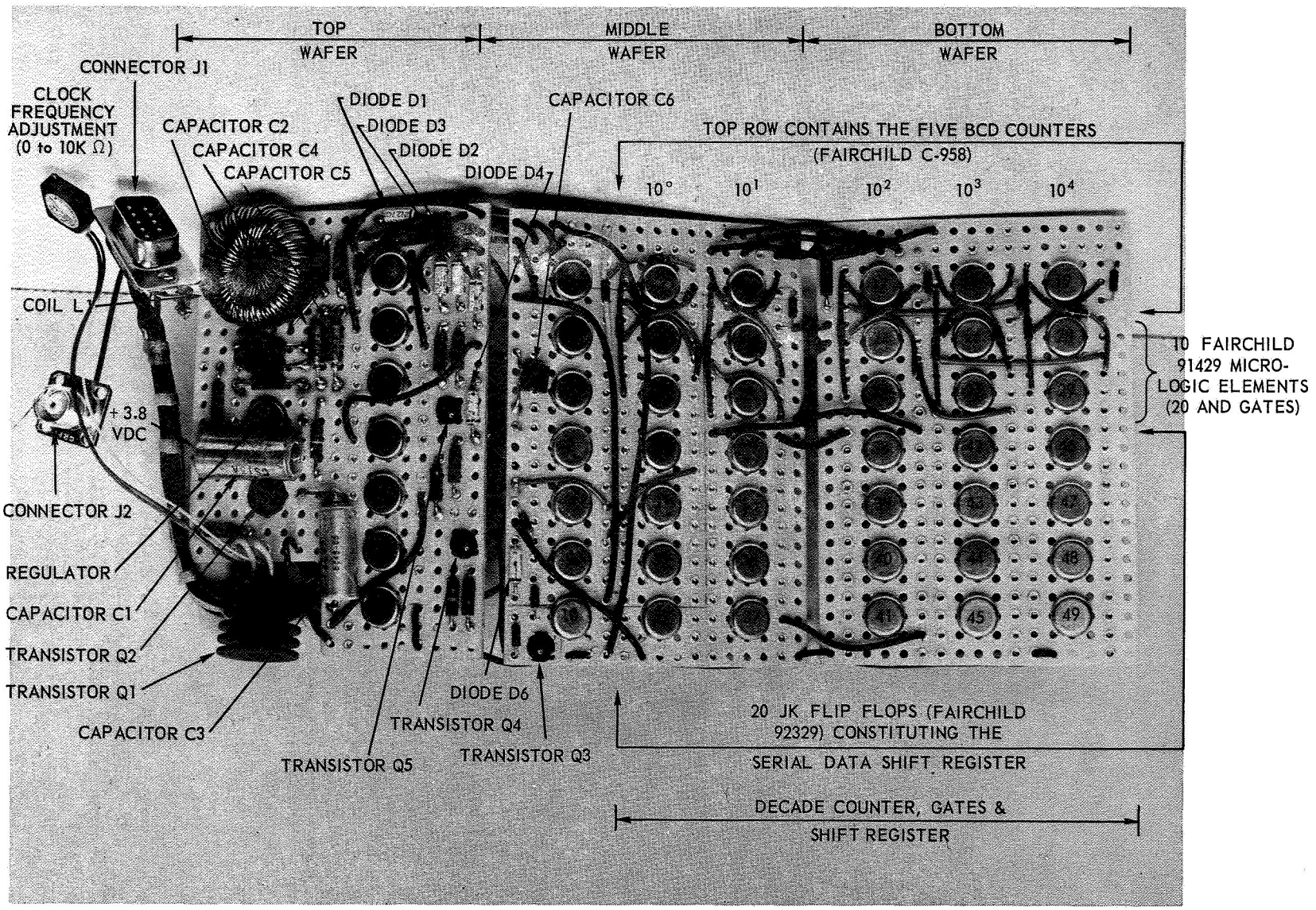


Figure 5. Board Assembly Layout, Component Side

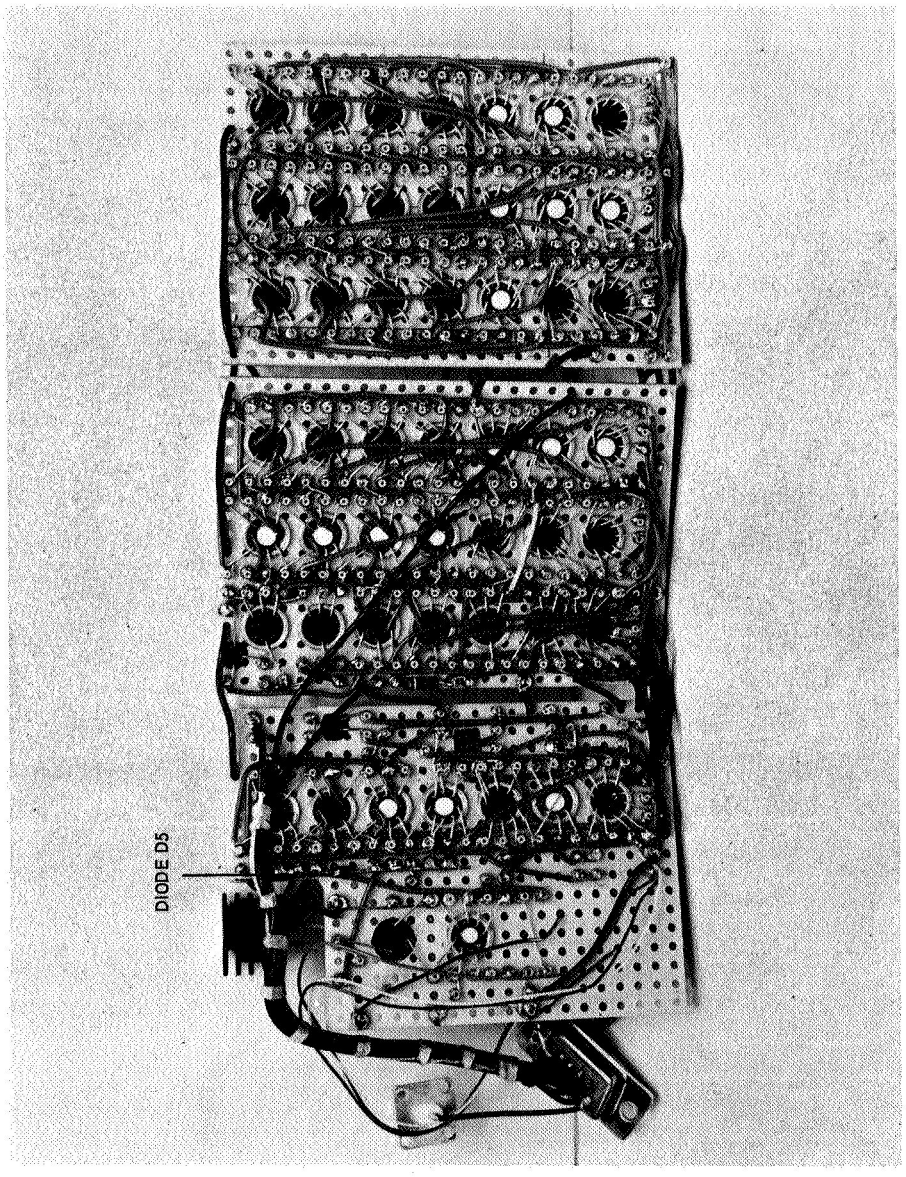


Figure 6. Board Assembly Layout, Wiring Side

The 25-hertz BIT pulses and (through inverter I1) the 5-hertz CHARACTER SPACE pulses are applied to AND gate G2. In the gate, the BIT pulses inhibit the CHARACTER SPACE pulses for 60-milliseconds out of every 200 milliseconds to produce the SHIFT waveform. The SHIFT waveform consists of sets of four 20-millisecond pulses spaced 20 milliseconds apart, with an interval between sets of 60 milliseconds. The primary use of the SHIFT waveform is to move the count, which is transferred instantaneously (in about 1 microsecond) once each second from the decade counters, through the shift register. A complete count is moved out of the shift register, after five sets of the four pulses of the SHIFT waveform have passed. This is accomplished in 940 milliseconds, or one second less the width of the TRANSFER pulse. The SHIFT waveform, or rather not-SHIFT ($\overline{\text{SHIFT}}$), is also used to establish the ZERO and SPACE (0.6 volt) levels of the output waveform through the output circuit. A third use of the SHIFT waveform is as one of two inputs, together with the COUNT OUTPUT waveform, to an AND gate consisting of transistor Q5 and diode D4. This gate provides the ONE (1.2 volts) level of the output format.

The 5-hertz CHARACTER SPACE pulses are also applied, through inverter I6 to three flipflops, modules 11, 12, and 13. These are connected (in modulo 3) to divide by 5 and produce a 1-hertz output. Once each second, a fourth flipflop, module 14, which is continually reset by the SHIFT pulses, is toggled to a ONE state by the 1-hertz waveform. The output of module 14 is the TRANSFER waveform, which consists of 60 millisecond pulses occurring every second. The primary use of the TRANSFER pulse is to move data in parallel fashion from the decade counters to the output shift register. Since input pulses to the counter-encoder can occur at a maximum rate approaching 1 every 10 microseconds, it is desirable that the transfer take place in minimal time. To accomplish this, the ONE output of module 14 is differentiated to reduce the 60-millisecond interval of transfer to a time of transfer of approximately 1 microsecond. The full 60-millisecond width of the TRANSFER pulse is applied from the ZERO output of module 14, through inverter I7 to the output circuit, where it serves to clamp the output at 3.2 volts and produce the output SYNC pulse. A third function of the TRANSFER pulse is to inhibit input gate G1 to the decade counters during the instant of transfer.

In summary, the output format is made up of timing pulses briefly described as follows. BIT pulses occur once every 40 milliseconds. SHIFT pulses occur four times every 200 milliseconds establishing, (1) a ZERO output level to indicate the absence of a data bit, (2) a SPACE (0.6 volts) level indicating a space between bits, and (3) a ONE level indicating the presence of a data bit. CHARACTER SPACE pulses appear in the output format four times a second at the SPACE (0.6 volt) level to indicate a separation between characters. A fifth CHARACTER SPACE pulse and the TRANSFER pulse occur in coincidence with

the SYNC pulse, which appears once a second, at the 3.2 volt level of the output format. (See Figure 7.)

THE COUNTER

The purpose of the counter is to receive periodic or random pulses, occurring at a maximum rate of less than 100 kilohertz, and, even during the transfer time, to count them every second. The counter consists of an input buffer amplifier, an input flipflop, an exclusive OR gate, inverters, an AND gate, and five decade counters. Except for the decade counters, all of the above devices and the first flipflop (least significant bit) of the first decade counter (units decade) are associated in an input circuit, the purpose of which is to ensure that an input pulse will be counted unambiguously, even when it occurs at the instant of transfer.

Except during the instant of transfer, a voltage from the integrator at the ONE output of module 14 maintains AND gate G1 in an enabled condition. When the input flipflop and all of the flipflops in the decade counters are reset, all flipflops in the counters and the input flipflop are returned to the same zero condition. The first input pulse causes a signal to follow a route through the buffer amplifier, the input flipflop, the exclusive OR gate, inverter I1, AND gate G1, the first flipflop of the UNITS decade counter, inverters I4 and I3, and back to the exclusive OR gate which it closes. All additional input pulses follow the same route. An input pulse occurring at the instant of transfer, when AND gate G1 is disabled by a voltage from the integrator, will not pass through the gate, but will be retained by the input flipflop until the approximately 1 microsecond period has passed, at which time the gate will open and the pulse will follow the established path. Thus the input circuit ensures that each pulse will be counted and that it will be counted only once, and only within the one-second interval in which it occurs.

Each of the five decade counters are identical, and conventional, in that they are internally connected to reset to zero and transmit a carry signal to the next-more-significant counter when the binary count reaches the decimal equivalent of 9. Resetting all counters to zero is accomplished by an additional pulse after a count of 99,999, or by an external reset pulse, and is independent of the one-second samplings of the count. Thus a complete count can be made in a minimum period of one second or in an indefinitely long period of time.

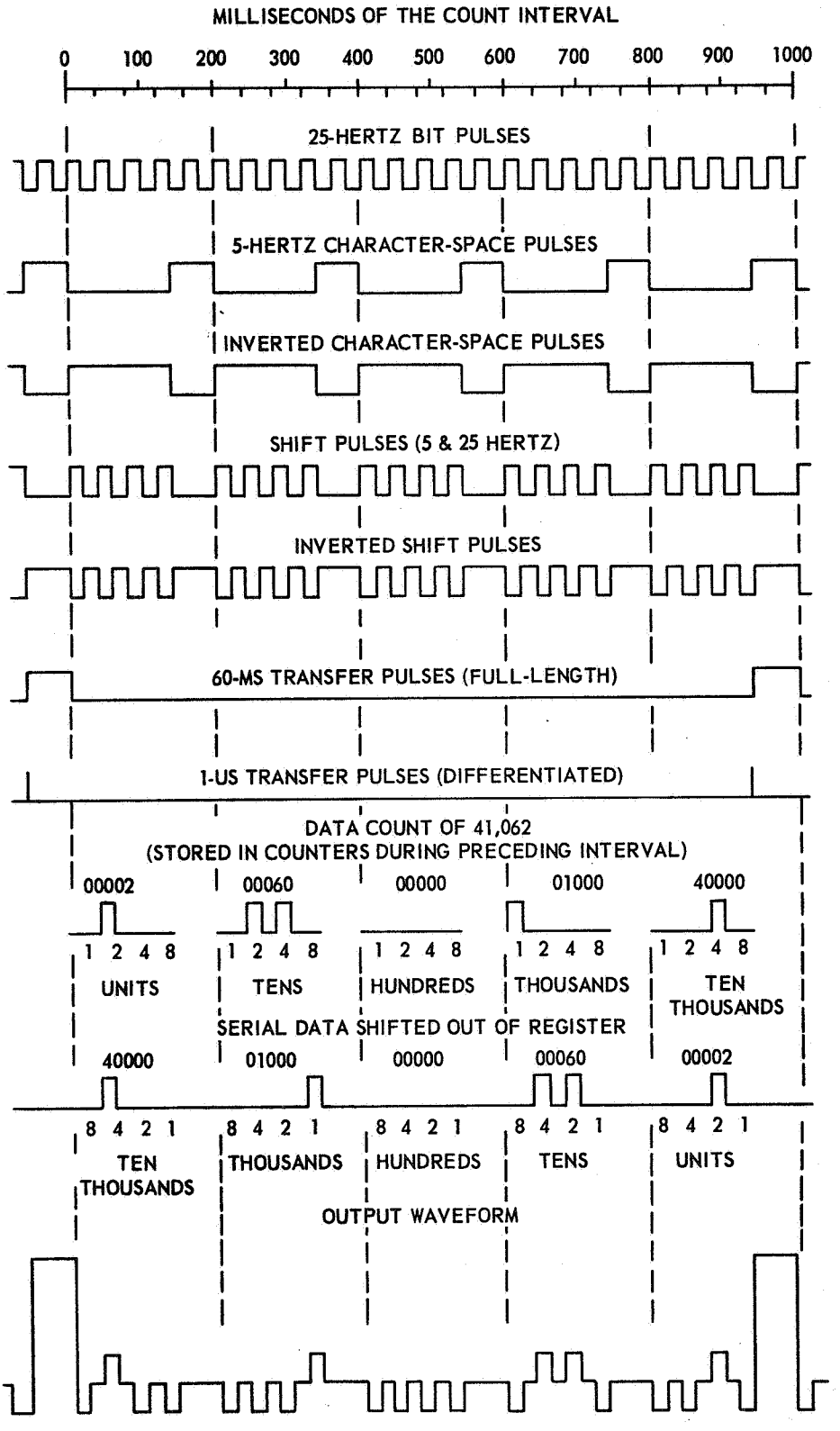


Figure 7. Counter-Encoder Timing Waveforms

THE ENCODER

The encoder consists of twenty AND gates and a shift register composed of twenty flipflops. The AND gates are simultaneously enabled once a second by the 1-microsecond TRANSFER pulse. They serve to set the twenty flipflops in the shift register to the condition, at the instant of transfer, of associated flip-flops in the five decade counters. After transfer, and for most of the one-second interval, the count is driven out of the register by, and in the format of, the SHIFT pulses to the output circuit.

THE OUTPUT CIRCUIT

The function of the output circuit is to provide the voltage levels of the output format, and to provide an isolated output signal at pin 1 of connector J1. The circuit consists of three channels which are combined in a diode OR gate and amplified in an emitter follower. Inverters I5 and I7 through I10, and an AND gate composed of transistor Q5 and diode D4, also form a part of the output circuit.

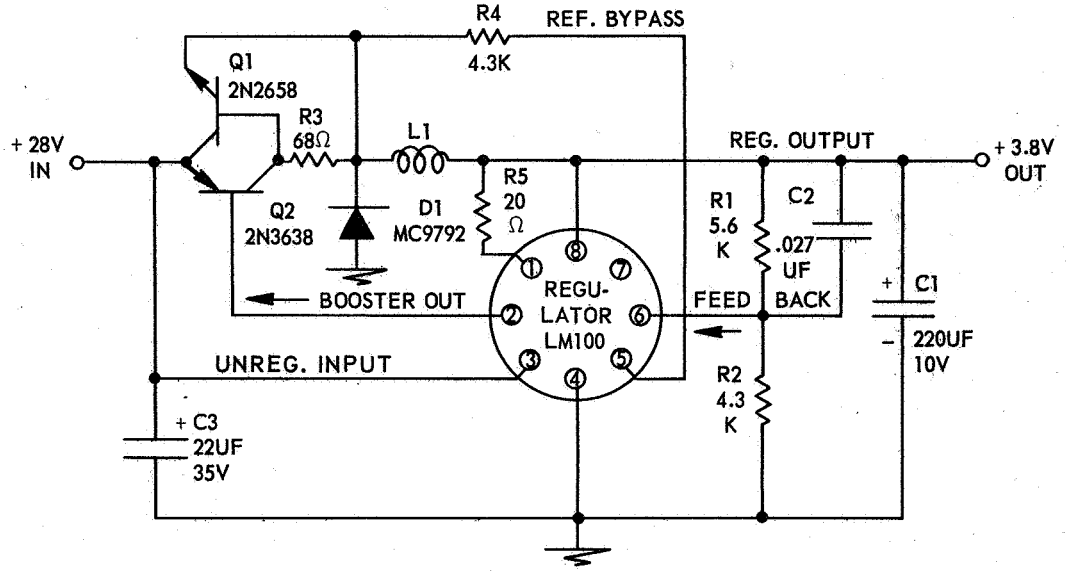
Negative-going formatted data pulses from the shift register are coupled through diode D4 to the collector of transistor Q5. During data intervals, the base of Q5 is regularly driven toward ground potential by bit pulses of the inverted SHIFT waveform ($\overline{\text{SHIFT}}$). The effect of this bias is nil unless a negative-going data pulse is also at the collector of Q5. The coincidence of both pulses, however, cuts off conduction in transistor Q5 abruptly, and a positive pulse of approximately 1.2 volts in amplitude, at the ONE level of the output format, is coupled through OR gate diode D2.

Inverted SHIFT pulses ($\overline{\text{SHIFT}}$) are also applied to OR gate diode D3. These are coincident with BIT SPACE pulses, and serve to establish the ZERO level of the output format at approximately 0.6 volt.

Full-width TRANSFER pulses, 60 milliseconds long, are applied to diode D1 of the output OR gate. These serve to establish the SYNC pulse of the output format at a level of approximately 3.2 volts.

POWER SUPPLY

The power supply consists of a switching regulator which is mounted on one of the boards of the counter-encoder (Figure 8) and an external battery pack. The battery pack provides an unregulated input voltage of approximately



NOTES: 1. L1 consists of a magnetics #55204-A2 core upon which 200 turns of #22 copper wire are wound.

2. The regulator is an NSC#LM100 integrated regulator. Terminals are shown as seen from the top. Pin 4 is connected to the case.

Figure 8. Power Supply Schematic Diagram

+28 volts d.c. The switching regulator converts this voltage into a steady +3.8 volts d.c. to provide power for all circuits of the counter-encoder.

The regulator consists of a National Semiconductor Corporation LM100 voltage regulator, and other components arranged in the circuit, as shown in Figure 8. Switching-output voltage changes are coupled through capacitor C2 to terminal 6 of the LM100 regulator. Regulating control is applied from pin 2 to the base of driver transistor Q2, which controls the operation of chopping-transistor Q2. The chopping frequency is approximately 10 kilohertz, with a duty cycle of 17 percent. Filter L1-C1 maintains the ripple voltage at about 60 millivolts, peak-to-peak. Efficiency is approximately 75 percent. Under full load, the power supply will operate within a temperature range of 0°C to 70°C (32°F to 158°F).

CLOCK FREQUENCY ADJUSTMENT

The counter-encoder clock frequency is adjustable from the normal rate of 50 hertz to maximum and minimum rates of about 75 and 35 hertz. Timing components can be changed to provide a different range, if desired. The logic circuitry will function at almost any clock rate. If a different clock rate is used, the output format will simply be stretched, or compressed, according to the clock frequency selected.

RESETTING THE COUNTERS

It is necessary to initially reset all counters to ZERO before proper counting action can occur. External resetting of the counters is accomplished when +28 volts d.c. is applied to the EXTERNAL RESET (pin 2 of connector J1) lead for at least 1 microsecond (Figure 4). The reset signal must be removed before counting can occur. Once reset, the counters will remain in the reset condition until the first input pulse is received.

APPLICATION

The new digital accelerometer, with which the counter-encoder is to find immediate application, is shown in Figure 9. This device is unipolar in that it senses accelerations, for example, in the forward direction, or in the reverse direction, but not in both directions at same time. It produces an output of 20-volt, 10-microsecond pulses at a rate of 32.2 pulses per second per g, in a range of 0 to +20 g's. It requires the same input voltage as the counter-encoder and consumes about a tenth as much power. Contained in a space of about 8.5 cubic inches and weighing 8 ounces, the accelerometer is slightly smaller and lighter than the counter-encoder. (See page 1.) Detailed specifications may be obtained from the manufacturer, the Systron-Donner Corporation of Concord, California.

The block diagram in Figure 10 shows the main elements, interconnections, and controls of the acceleration-measuring and telemetering system planned for the launching of the Anchored IMP (Interplanetary Explorer). The system measures forward accelerations of the third stage of the Delta launch vehicle from liftoff to orbit, that is, it will measure forward accelerations imparted by the thrusting of each stage.

The two pullaway connections shown in Figure 10 are to permit inhibiting the output of the accelerometer, and the resetting of the counter-encoder to zero. In the final countdown, the INHIBIT-ENABLE switch is placed in the INHIBIT

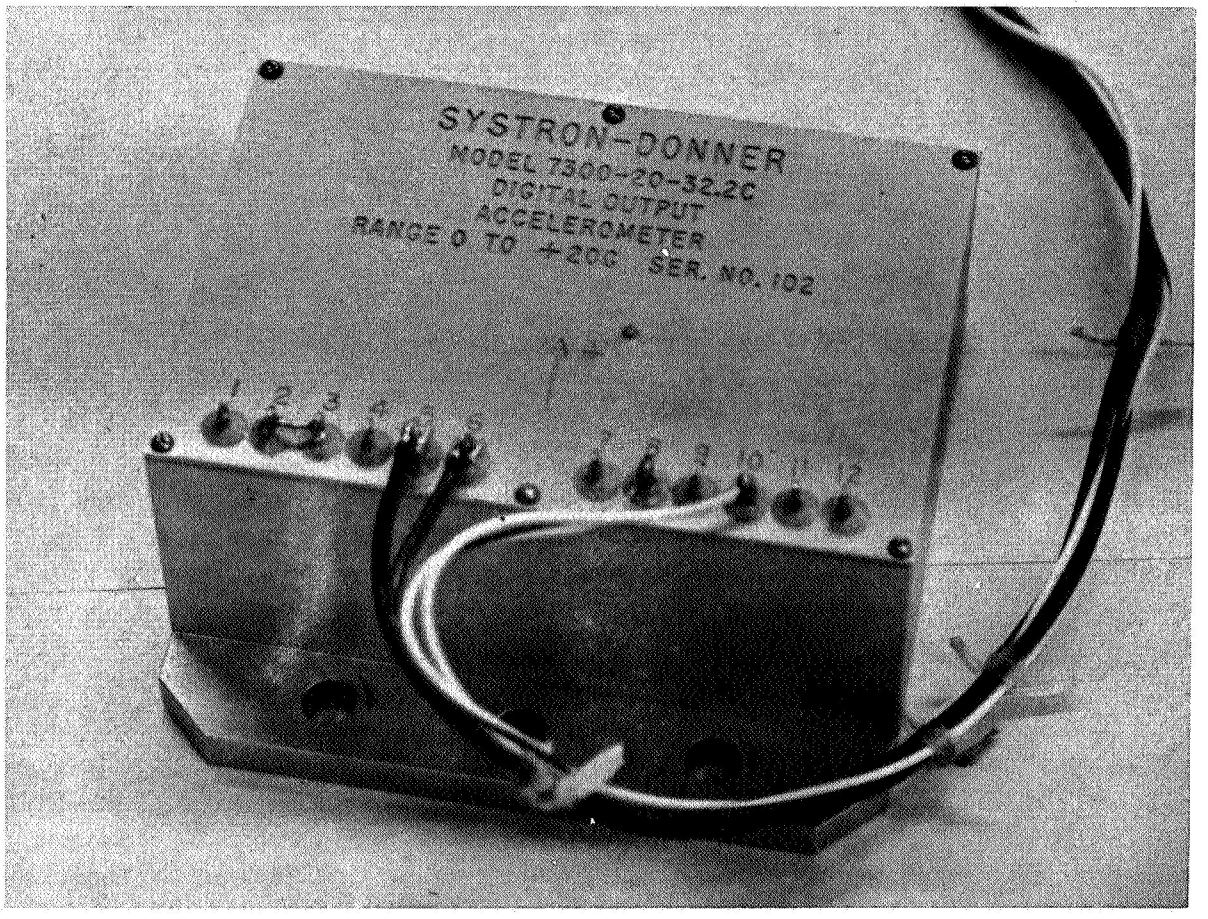


Figure 9. The Digital Accelerometer

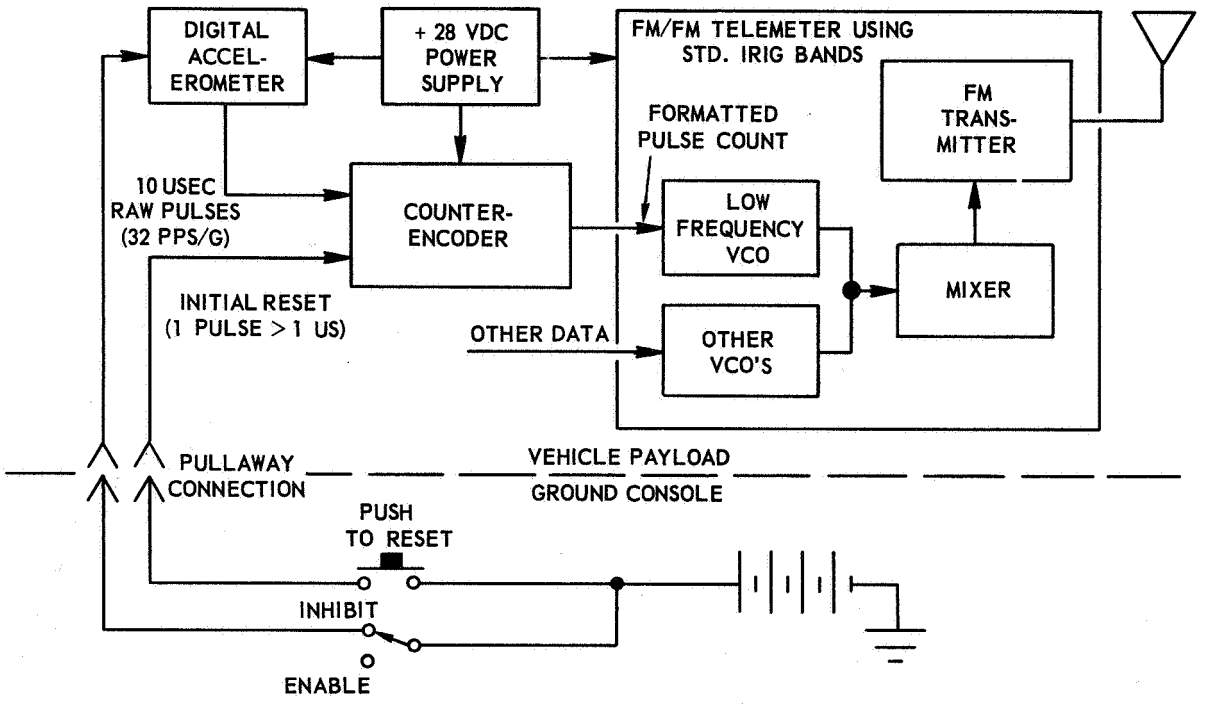


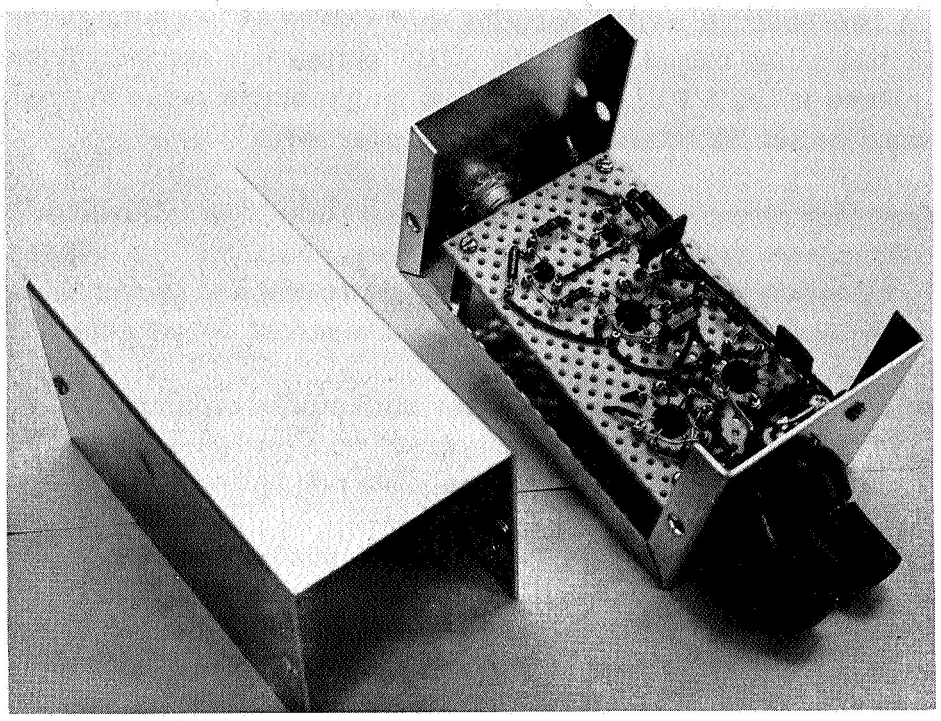
Figure 10. Application of the Counter-Encoder in the Anchored IMP Launch Vehicle

position to prevent the accelerometer from counting the lg acceleration due to gravity, and is left in this position until the vehicle leaves the launch pad. Before the end of the countdown the PUSH-TO-RESET button is pressed to reset the counter-encoder to 00,000. Separation of the pullaway cable at liftoff automatically enables the accelerometer by removing the inhibiting battery voltage from the ground console.

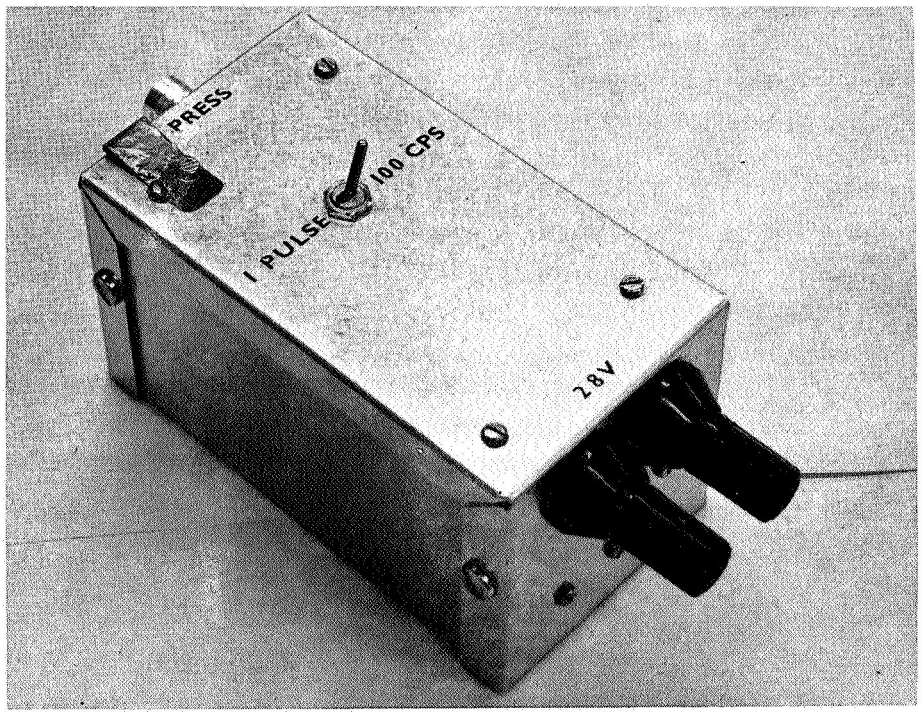
Since only forward accelerations are measured, and these only occur during the burning periods of three stages, the total accumulated count from liftoff to orbit is limited. The nominal burning times and peak accelerations of the Delta vehicle indicate the total accumulated pulse count to be less than the counting capacity (99,999) of the counter-encoder. This means that the counter-encoder will not reset itself during the time of interest, that is, the launch phase of the flight.

COUNTER-ENCODER TEST UNIT

A test unit, designed to provide a means for bench and field testing of the counter-encoder is shown in Figure 11. This device produces 10-microsecond pulses, approximately 20 volts in amplitude, to serve as an input to the counter-



A. Cover Removed



B. Cover Installed

Figure 11. Counter-Encoder Test Unit

encoder. A two-position switch permits selection of either a single-pulse output or a continuous-pulse output, at a rate of 100 pulses per second. When this switch is placed in the 1 PULSE position, a single output pulse is produced each time a second switch S2, marked PRESS, is pressed.

The test-unit circuits consist of three Fairchild RTL micrologic elements, two transistors, two switches, two zener diodes, and resistors and capacitors. It is easily assembled on a perforated phenolic board, and is conveniently housed in a standard minibox container which serves to mount the switches.

A block diagram, with waveshapes for both modes of operation, is given in Figure 12. The three micrologic elements serve as a 100-hertz multivibrator, a flipflop, and as a 10-microsecond one-shot multivibrator.

When switch S1 is in the 1 PULSE position, switch S2 and the flipflop are operative in the circuit. Each time switch S2 is pressed, voltage is applied to cause the flipflop to change from one stable state to the other and, through switch S1, to trigger the one-shot, causing it to produce an output pulse which is amplified by transistors Q1 and Q2.

When switch S1 is in the 100-hertz position, the 100-hertz multivibrator and the one-shot are operative. The output of the multivibrator changes to positive every 10 milliseconds, thus triggering the one-shot, and causing amplified pulse to appear at the output connector. The repetition rate may be varied by substituting different values for capacitors C2 and C3.

The unit requires a 28-volt-dc power input. The circuit formed by resistor R4, zener diode D1, and capacitor C1 provides a filtered, series-regulated voltage of 3.9 volts dc for the micrologic elements and transistor Q1.

The test setup is shown in Figure 13. After the ground station equipment has been set up to produce a paper record and all equipment in the test setup has been energized, switch S1 of the test unit is placed in the 1 PULSE position. The PUSH TO RESET button in the test setup is then pressed to return any count in the counter-encoder to zero. Next, switch S1 of the test unit is placed at 100 PPS, and the ground station record is examined to determine that the BCD output of the counter-encoder indicates count increments of 100 for each second after switch S1 was placed at 100 PPS. When this is verified, switch S1 is placed in the 1 PULSE position, switch S2 is depressed a counted number of times, and the count is read from the record. If the count of the number of times that switch S2 is pressed agrees with the number recorded, satisfactory performance of the counter-encoder is confirmed.

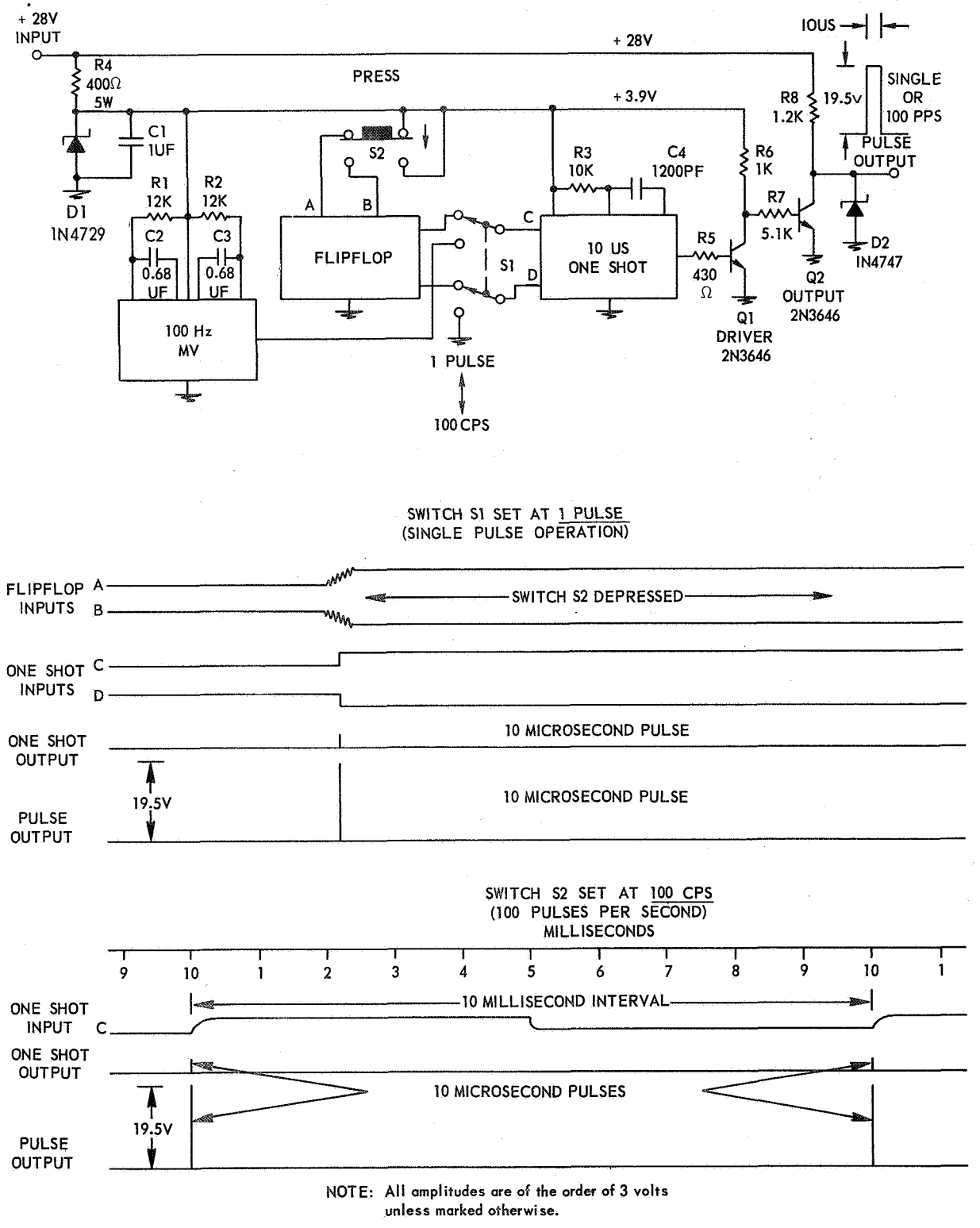


Figure 12. Block Diagram and Waveforms of the Counter-Encoder Test Unit

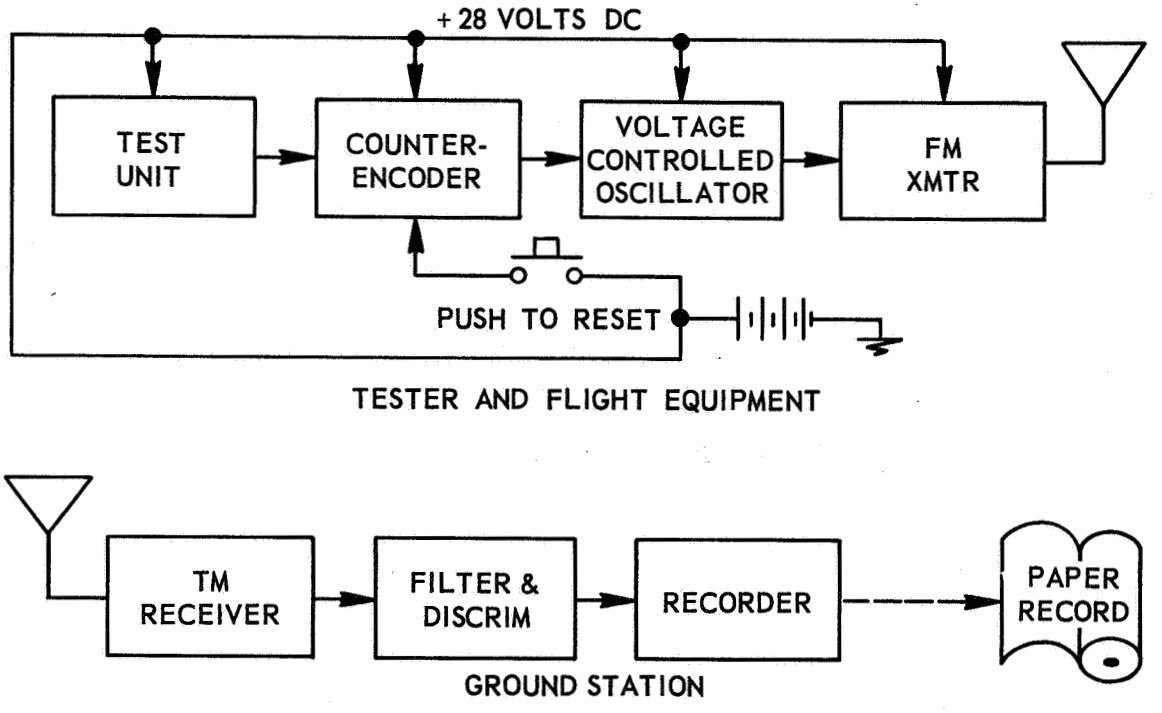


Figure 13. Counter-Encoder Test Setup

APPENDIX

Summary of Specifications

SUMMARY OF SPECIFICATIONS

ELECTRICAL

External Power Required	+10 to +30 Vdc, 9 watts
Input Pulse Width	1 microsecond or greater; rise time of 50 microseconds or less
Maximum Input Pulse Rate	Approx. 100 kilohertz
Input Pulse Amplitude	+20 ±5 volts*
Output Pulse Amplitude	0 to +4 volts
Clock Rate	50 +25, -15 hertz*
Format Rate	1 ±0.25 hertz*

*A wide range of variation can be obtained by substitution of circuit components.

MECHANICAL

Length	3-1/2 inches
Width	2-1/2 inches
Width Including Protrusions	3-3/8 inches
Height	1-1/2 inches
Weight, Unpotted	7 ounces
Weight, Potted	13 ounces
Volume	13-1/8 cubic inches
Random Vibration, All Axes	20-2000 hertz, 6.15g rms
Sinusoidal Vibration, All Axes	400-2000 hertz, 5g maximum
Altitude	No Limit
Temperature	0°C to 70°C (32°F to 158°F)